REMARKS:

Applicants have carefully studied the Final Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicants respond to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Claim Rejections – 35 U.S.C. § 103

Applicants acknowledge the quotation of 35 U.S.C § 103(a).

Claims 1-24 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Regarding independent claim 1, the Office states that the AAPA discloses a method for transferring information to a bus comprising transferring the information (i.e., said information CAD, CDW, and CCO in said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed at page 9, paragraph [0029] of the specification as filed. Applicants respectfully disagree with the finding of the Office.

The specification of the instant application states at paragraph [0029] that information is transferred from the buffer to the bus after receiving a grant indication. As such, the AAPA teaches the step of transferring information from the buffer to the bus when the bus grant indication indicates that transfer of the information to the bus is allowed. Claim 1 has been amended to more clearly describe that which the applicants regard as the invention. Claim 1 previously included the step of transferring information to the bus when the buffer is empty and the transfer of information to the bus is allowed. Without reading limitations from the specification into the claim, the language of the claim as originally filed indicated that the

information is transferred to the bus, not to the buffer, when the buffer is empty and the transfer of information to the bus is allowed. Additionally, in the present invention, the transfer occurs when the buffer is empty, so information is not transferred from the buffer to the bus as in the AAPA reference. As such, the buffer is bypassed and information is transferred directly to the bus. The specification clearly supports this claim interpretation. Additionally, it is apparent that the Office has already interpreted the original language of claim 1 to indicate that the buffer was bypassed and information was transferred directly to the bus when the buffer is empty and the grant indication indicated that information to the bus was allowed as evidenced by the statement at Pg. 17, lines 2-5, of the Final Office Action in which the Office states, "In other words, memory read data is directly transferred from main memory to CPU/Cache bus without using RD buffer (i.e. bypassing buffer) if said RD buffer is empty and said CPU/Cache bus is available to be used (viz., bus idle) for transferring read data into CPU/Cache (i.e. allowed). However, to more clearly describe the invention, claim 1 has been amended to expressly state that in accordance with the present invention, the information bypasses the buffer and is transferred to the bus when the buffer is empty and the transfer of the information to the bus is allowed.

For the reasons cited above regarding amended claim 1, Applicants do not believe that the AAPA teaches the step of bypassing the buffer and transferring the information to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed. What AAPA does teach is the method step of transferring the information from the buffer to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed. As such, the buffer is not bypassed in the AAPA, but is rather used in the transfer process.

The Office states that the AAPA does not teach transferring the information to the bus if the buffer is empty and the transfer of information to the bus is allowed, but that Park discloses a method for a cache line replacing system, wherein said method for reducing latency in information transfers to a bus includes transferring information (i.e., line of cache data) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD Buffer 36 of Fig. 3) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46). Applicants respectfully disagree with the finding of the Office.

The Office contends that the statement, "transfer of the information to the bus is allowed", is equivalent to the claim language which states, "the bus grant indication indicates that transfer of the information to the bus is allowed". Just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, this does not mean that transfer of information to the bus is allowed as claimed by the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the transfer of information to the bus is allowed. Simply because the bus is idle does not mean that transfer of said information to the bus is allowed, there may be other bus requests waiting to be serviced. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that specific information is allowed to the transferred to the bus. This "allowance of transfer" is not equivalent to the bus being idle and "available for transfer".

Additionally, the Office states at Pg. 19, beginning at line 7, that Park discloses that the read data is transmitted with regard to the status of the CPU/Cache bus. Applicants disagree with this statement by the Office. Applicants contend that the read data is transmitted to the CPU/Cache bus with regard to the count value register, not with regard to the status of the CPU/Cache bus. As stated in Col. 5, lines 25-30, after all of the data stored in the read buffer has been read, that is the count value of the buffer count register becomes zero, the multiplexer switches over to connect the memory bus and data of the memory bus is transmitted directly to the CPU/Cache bus. The Park reference does not discuss the use of any type of bus grant request system to track the status of the CPU/Cache bus. In the Park reference, the CPU/Cache bus is always available for access by the cache buffer or the memory bus. Park does not discuss the need for a bus grant to access the bus because apparently the bus is always available when it is not being used. It can be inferred that the CPU/Cache bus is a dedicated bus and therefore bus grant requests and the issuance of grants are not necessary with the Park system.

At the bottom of Page 17 and the top of Page 18 of the Final Office Action, the Office summarizes its opinion by stating that Park clearly suggests the claimed limitation of, "transferring the information to the bus if the buffer is empty and the transfer of the information

to the bus is allowed", and that while Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer, that the AAPA teaches such a limitation. As such, the Office relies on the combination of the buffer status as taught by Park with the bus grant indication as taught by the AAPA to arrive at the invention.

Applicants believe that the Office's obviousness rejection is defective due to the inclusion of separate references to represent each of the different features described in the claims of the application. In fact, the Office has created features that do not exist in the claims by improper division of the claim language. With specific regard to claim 1, Applicants contend that the Office has lost site of the claim as a whole and is attempting to piece together the claimed invention using the claims as a guide. The Office has taken the claim language of one of the claim limitations of claim 1 and separated it into pieces, then identified references that the Office believes teaches each of the pieces individually and then pieced the pieces back together to arrive at the claim language. More specifically, the Office has taken the claim element which states, "transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed", and separated it into two distinct elements, which include, "transferring the information to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed", and "transferring the information to the bus if the buffer is empty". However, the claim as a whole does not provide these two distinct elements. In contrast, the claim language combines these two elements with a conjunctive "and" indicating that both conditions are required for the transfer of information. In other words, the claim language of claim 1 indicates that bypassing the buffer and transferring information to the bus occurs when the buffer is empty **and** the bus grant indication indicates that transfer of the information to the bus is allowed. Additionally, the Office has divided the claim element even more by breaking apart the element which states, "transferring the information to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed", by addressing the use of a bus grant indication separately from the allowance of information transfer to the bus. By separating this statement, the Office has improperly interpreted the claim. The claim element depends upon the bus grant indication indicating that the transfer to the bus is allowed. Separating the bus grant indication from the element is improper and results in a misinterpretation of the claim language. In particular, the Office cites the Park reference to support bypassing the buffer and transferring information to the bus and the

AAPA reference to support the use of a bus grant indication to indicate that the transfer of information to the bus is allowed. However, the claim element states, "transferring the information to the bus **if** the bus grant indication indicates that transfer of the information to the bus is allowed". Clearly, the transfer of the information to the bus depends upon the bus grant indication as is evidenced by the use of the term "if" in the claim element. As such, it is improper to divide the claim element as presented by the Office and in so doing, the Office has lost site of the claim as a whole.

Another issue before the Office is whether it would have been obvious to combine the references without having access to the application that is under examination to arrive at the claimed invention. In support of the combination of references, the Office states on Pg. 4 that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, the advantage of providing a way that a device (i.e. CPI) can read said information (i.e. data) at high speed without loss of said bus bandwidth (i.e. memory bus bandwidth; see Park, col. 6, lines 30-31). Applicants respectfully disagree with the determination by the Office regarding the combination of references.

Park teaches transferring information to the bus when the buffer is empty and the bus is "available", not that the transfer of the information to the bus is "allowed", which are two different things as explained above. The AAPA teaches the use of a bus grant indication to indicate that transfer of the information to the bus is "allowed". The Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest the step of transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed.

Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Regarding independent claim 9, the Office states AAPA teaches logic configured to cause the information to either be stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the buffer to the bus if the bus grant indication indicates that transfer of the information from the buffer to the bus is allowed. However, the claim element of amended claim 9 states that the information be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. As such, AAPA teaches transferring information from the buffer to the bus dependent upon the status of the bus grant, but AAPA does not teach transferring information from the device to the bus without passing through the buffer.

Additionally, the Office states AAPA does not teach logic being configured to cause the information to be transferred from the device to the bus if the buffer is empty and the transfer of the information to the bus is allowed, but that that Park does disclose logic configured to cause information to be transferred from the device to the bus if the buffer is empty and transfer of the information to the bus is allowed. The Office cites the MUX **38** and Buffer WT Reg **37** of Fig. 3 in support of this statement. Additionally, the Office states that the CPU/Cache bus is idle after the write-back data is stored in the write-back buffer and as such, the transfer of the information to the bus is allowed.

Applicants respectfully disagree with the finding of the Office. As detailed with regard to independent claim 1, just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, does not mean that transfer of information to the bus is allowed, as claimed by the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the transfer of information to the bus is allowed. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that specific information is

allowed to be transferred to the bus. This "allowance of transfer" is not equivalent to the bus being idle and "available for transfer". For the reasons cited above, Applicants contend that Park does not describe logic configured to cause information to be transferred from the device to the bus if the buffer is empty and transfer of the information to the bus is allowed.

The Office concludes with regard to independent claim 9 that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic, as disclosed by Park, in said logic as disclosed by AAPA, for the advantage of providing a way that said device can read information at high speed without loss of said bus bandwidth.

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

Regarding independent claim 19, the Office states that AAPA does not teach a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer having first inputs coupled to the inputs of the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus. However, the Office goes on to state that Park discloses a cache line replacement apparatus, wherein a buffer bypass circuit for reducing latency in information transfers to a bus comprising: a multiplexer having first inputs coupled to inputs to a buffer; second inputs coupled to the outputs of the buffer; outputs coupled to the bus; at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of

the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

Applicants respectfully disagree with the conclusion of the Office. Claim 19 of the present invention includes, "at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus." As such, the control information couples the first inputs of the multiplexer to the outputs of the multiplexer, which are coupled to the bus, if the buffer is empty and the bus is available for transfer of the information to the bus. The Office states that Park teaches that the bus is available for transfer of the information to the bus, as supported by col. 3, lines 27-35, and col. 4, lines 31-46, in which the CPU//Cache bus is idle after write-back data having been stored in write-back buffer. As detailed with regard to independent claim 1, just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, does not mean that the bus is available for transfer of "the" information to the bus, as claimed by the present invention. The availability of the bus is determined by the grant indication of the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the bus is available for transfer of the information to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that the bus is available for the transfer of identified information to the bus. For the reasons cited above, Applicants contend that Park does not describe logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said buffer bypass circuit, as disclosed by Park in said logic, as disclosed by AAPA, for the advantage of providing a way that said device can read said information at high speed without loss of said bus bandwidth.

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that the bus is available for transfer of the information to the bus. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

For the reasons cited above, Applicants believe that independent claim 1 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 2-8 are dependent upon claim 1, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 9 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 10-18 are dependent upon claim 9, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 19 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 20-24 are dependent upon claim 19, and are therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned is requested.

Respectfully Submitted,

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Date

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